Modelling & Simulation
Logic Simulation

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Logic simulation

- = digital simulation, digital circuits simulation
- simulates operation of logic systems
  - logic system = logic circuit = digital circuit
    - signals are represented by discrete bands of analog levels
- Used for
  - design & development
    - to validate/verify the design
    - at different levels of abstraction
  - diagnostics
    - to check completeness of tests
      - Simulation with/without known errors

Levels of logic circuits design

Level	Systems	Elements	Signal units
Electronic System Level (ESL)	Computer systems	CPU, memory, I/O devices, channels,...	word blocks
Register transfer level (RTL)	CPU, ALU, memory,…	register, coder, decoder	words *(sequences of bites)*
Gate level (Logic circuits level)	register, coder, counter	gates (and, or,…), flip-flops(D, JK,…)	bites
Electronic circuit l. (Transistor level)	gates, flip-flops	transistor, diode, capacitor, …	voltage levels
Physical level	transistor, diode, resistor	diffusion areas, contacts	-(physical dimensions)

Levels & logic simulation I

- Not a logic simulation:
  - Electronic system level (ESL)
    - = behavioural level
    - as queuing systems
  - Electronic circuit level
    - utilises electrical laws (Kirchhoff's, Ohm's)
    - dynamic behaviour – equations (differential)
    - continuous systems
  - Physical level

Levels & logic simulation II

- Belongs to logic simulation:
  - RTL
  - Gate level
  - Distinction between these levels is not that clear
    - often mixed in designs
    - simulation at several levels at once is possible
  - Models of elements
    - mathematical (esp. at gate level): Boolean algebra, finite automata
    - behaviour often described in VHDL
- Logic simulation = a special case of discrete simulation

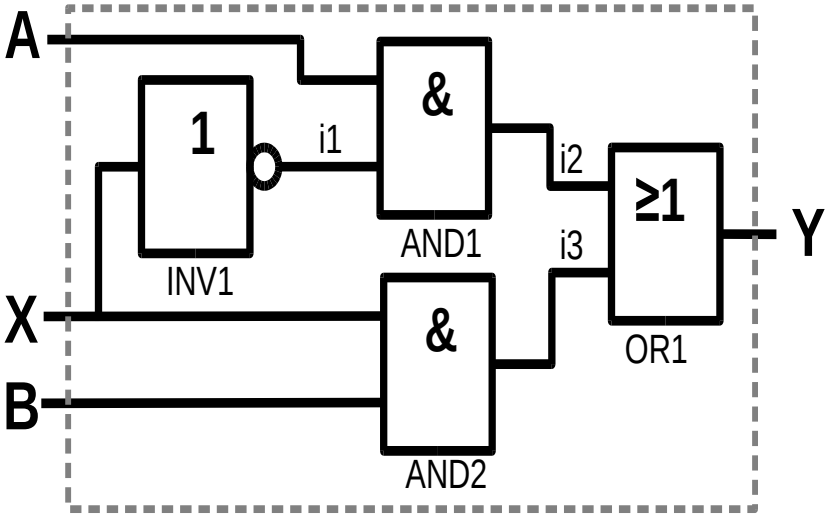
Modelling of digital circuits

- Modelling languages
- Signal models
- Timing models
- Fault models

Modelling languages

- Describing only structure
  - Fixed library of elements (gates, flip-flops, registers,…)
  - elements can be parameterised
- Describing structure and behaviour
  - Can define new elements
    - inputs, outputs + behaviour in the language
  - GPPLs can be used
  - Hardware description languages: VHDL, Verilog
- Hierarchical design
  - New elements defined by existing ones

Model examples (2-to-1 1 bit multiplexer)




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux_2to1 is
 Port ( A : in   STD_LOGIC;
        B : in   STD_LOGIC;
        X : in   STD_LOGIC;
        Y : out  STD_LOGIC );
end mux_2to1;

architecture Behavioral of mux_2to1 is
begin
    Y <= A when (X = '0') else B;
end Behavioral;
```

$$Y = (A \cdot \overline{X}) + (\mathrm{B} \cdot \mathrm{X})$$

Signal models

- L, H
  - L = low (0); H = high (1)
- L, H, u
  - u (or X) = undefined, unknown (0 or 1)
    - to model unknown states (i.e. of flip-flop after powered up) or some kinds of hazards (oscillations)
- L, H, u, Z
  - Z = high impedance
    - third value of tristate gates
- L, H, u, R, F
  - R = rise (0→1)
  - F = fall (1→0)
- Additional values for hazards
- Simulation of MOS Digital Circuits
  - strong/weak L, H

Note:: hazards

- undesirable effects of delays
- Static hazard
  - Static-1
    - the output is currently 1 and after the inputs change, the output momentarily changes to 0 before settling on 1
  - Static-0
    - vice versa
- Dynamic hazard
  - possibility of an output changing more than once as a result of a single input change.

Timing models

- zero-delay model
  - no delay
  - only functional simulation
- unitary delay
- delay set as one value
- delay set as interval (min, max)

Fault models

- To simulate faults in circuits when the simulation is used to evaluate diagnostic tests.
- At gate level
  - Single stuck line fault model
    - Stuck at 0 – the given signal is always 0
    - Stuck at 1 – the given signal is always 1
    - assumes that only one input on one gate will be faulty at a time
    - works well for TTL, moderately well for CMOS
  - short circuit between signal wires
- At RTL
  - a fault represents a group of faults from lower level
  - memory faults, control faults, decoder faults,…

Logic Simulation Methods

- Compiled-code simulation
- Event-driven simulation

Compiled-code simulation

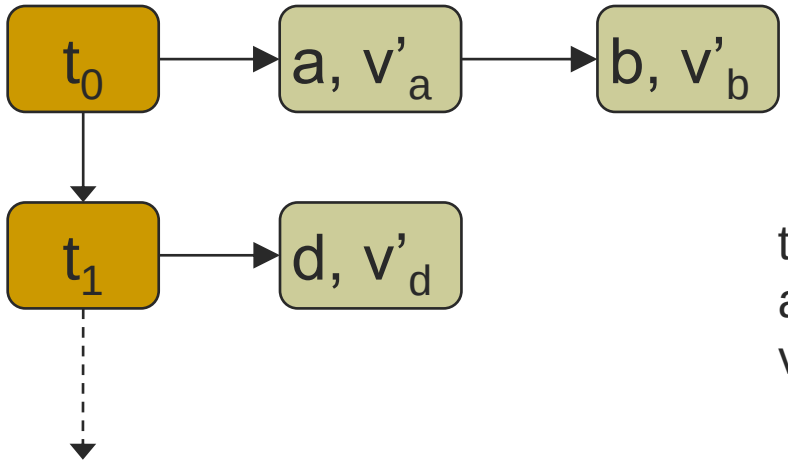
- The digital circuit model is translated into a series of machine instructions that model the functions of individual gates and the interconnects between them.
- Incapable of timing modelling
  - zero-delay model
  - most effective for L, H signal model
    - machine instructions directly useable
- Used for cycle-based simulation

Event-driven simulation I

- Highly efficient
  - evaluates gates only when necessary
- Event
  - = switching of a signal value
- Event-driven simulator
  - monitors occurrences of events to determine which logic elements to evaluate
- Can handle any delay model
  - by means of event scheduler

Event-driven simulation II

- Event scheduler
  - Implemented as priority queue



t_0,t_1 – timestamps
a – signal a
v'_a – new value of signal a

Logic Simulation Software

- Commercial
  - Matlab
  - TINA
  - Mentor Graphics FPGA Advantage
- Free
  - Deeds
  - Logsim
  - Qucs